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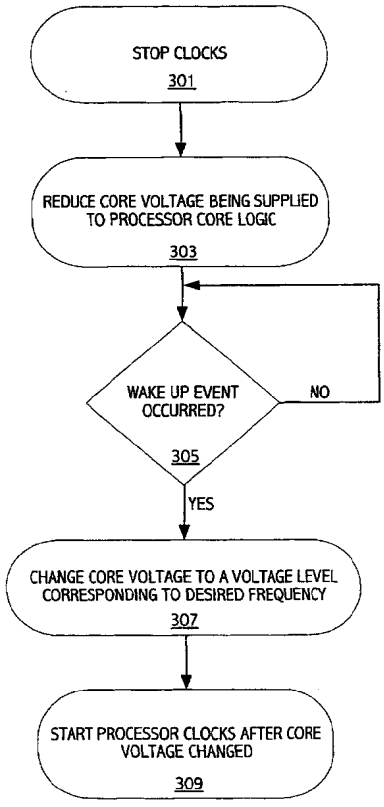
(54) Title: MINIMIZING POWER CONSUMPTION DURING SLEEP MODES BY USING MINIMUM CORE VOLTAGE NECESSARY TO MAINTAIN SYSTEM STATE



(57) Abstract: A control circuit reduces voltage being supplied to an integrated circuit in a sleep mode in which context (e.g. CPU state) is maintained. Because the voltage required to maintain the integrated circuit state intact may be significantly less than the voltage at which the integrated circuit can functionally operate at a predetermined frequency, significant power savings can be achieved by reducing voltage while the clocks are stopped, thereby reducing leakage current and saving power.

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MINIMIZING POWER CONSUMPTION DURING SLEEP MODES BY USING MINIMUM CORE VOLTAGE NECESSARY TO MAINTAIN SYSTEM STATE

Technical Field

This invention relates to power consumption in integrated circuits and more specifically to reducing power consumption on an integrated circuit while clocks are stopped.

Background Art

A conventional notebook computer has power constraints that cause it to employ techniques to reduce power consumption to conserve battery life. In addition, the conventional notebook computer has thermal constraints due to a small, densely packed system construction that limits its ability to safely dissipate the heat generated by computer operation. The power savings techniques also beneficially reduce the amount of heat needed to be dissipated.

The frequency of operation (clock frequency) of the processor and its operating voltage are primary determinants of power consumption. Since power consumption and dissipation are roughly proportional to the processor's frequency of operation, scaling down the processor's frequency has been a common method of staying within notebook computer power and thermal limitations.

A common power management technique, called "throttling", temporarily stops processor clocks, to reduce power consumption and thus reduce heat generation. Throttling continuously stops and starts processor operation by turning its clocks off and on according to a predefined duty cycle with a period of a few milliseconds. The reduction in the effective speed of the processor reduces power dissipation and thus the processor's temperature. A clock control signal (e.g., STPCLK# in x86 architectures) modulates the duty cycle of processor operation. The clock control signal, when asserted, causes the processor to gate off the clocks being supplied to core logic in the processor. In some current processor designs, e.g., x86 processors, a Stop Grant cycle on a host or system bus is executed to indicate that the stop clock request on the asserted clock control signal has been completed. A temperature sensor placed on or near the processor's heat sink can initiate throttling when needed.

In addition, when operating from its battery, most notebooks take advantage of the processor's idle periods by periodically stopping processor operation to reduce power consumption. Applications like word processors typically leave the processor idle much of the time. For example, in a word processing application, a processor will do a brief burst of work after each letter is typed, then its operation is stopped until the next keystroke. As a result, the typical processor power consumption when running a word processing application, can be as much as 30-50% below the maximum. That idle time can be exploited by the computer system to achieve additional power savings by putting the processor to sleep temporarily.

Current x86 based computer systems utilize an industry supported power management approach described in the Advanced Configuration and Power Interface Specification (ACPI), Revision 1.0a, by Intel, Microsoft and Toshiba dated November 19, 1998, which is incorporated herein by reference. The ACPI is an

operating system (OS) controlled power management scheme that uses features built into the Windows 95, 98 and Windows NT or other compatible operating systems. It defines a standard interrupt (System Control Interrupt or SCI) that handles all ACPI events. System control interrupts are generated by devices to inform the OS about system events.

As part of that power management approach, ACPI specifies sleep and suspend states. Sleep states temporarily halt processor operation and operation can be restored in a few milliseconds. A computer system processor enters the sleep state when internal activity monitors indicate no processing is taking place. When a keystroke is entered, a mouse moves or data is received via a modem, the processor wakes up in order to resume operation, the clocks are turned on and the CPU continues executing from where it left off.

Other modes save processor context external to the processor such as to system memory or even to hard disk. Suspend states shut down more of the notebook's system (e.g. display or hard drive) and take a few seconds for operation to be restored. Suspend states copy the present context of the system (sufficient for the computer to resume processing the application(s) presently opened) into memory (suspend to RAM) or to the hard drive (suspend to disk) and power down peripherals. Obviously in these other modes, longer latency is incurred to resume normal system operation.

When computer systems stop the central processing unit (CPU) clocks during a sleep mode or during throttling, a short latency for resuming processor operation is desirable. One way to achieve that short latency is to ensure that CPU context is not lost. That means that the various latches and other circuit nodes in the CPU that hold information required (e.g., the state of processor registers) for the processor to resume operations where it left off, are maintained in the CPU while clocks are stopped. Maintaining processor context requires that the CPU receive power even though the clocks are stopped.

Note that processors typically have separate regions of the chip that receive separate power supply voltages. For example, such regions may include a core region, as well as a peripheral region where input/output (I/O) circuits are located. The peripheral region often remains powered up even if the core voltage is turned off. Therefore, core voltage which must be maintained to ensure processor context is maintained (assuming I/O voltage is also on). In most current notebook designs, CPU core voltage is typically set during initialization, and is not changed after that.

When power is supplied during the sleep state to maintain CPU context, the CPU still consumes power because of leakage current. The leakage current is generally proportional to the core voltage, and the power consumption is proportional to the square of the core voltage. The leakage current can be significant enough to drain the battery. For example, an AMD-K-6®-2 processor can consume several hundred milliwatts while in sleep mode. Additionally, some circuit designs may be more leaky than others, resulting in even more power being consumed in sleep mode.

It is desirable to reduce power consumption in computers, particularly in portable computers where maximizing battery life and reducing heat generation by reducing power consumption is particularly

advantageous. Therefore it would be desirable to reduce power consumption, if possible, when clocks are stopped and power is being consumed due to leakage current.

DISCLOSURE OF INVENTION

Accordingly, the invention provides a way to save power while a processor (or other integrated circuit) is in a sleep mode in which context is maintained. Because the voltage required to maintain the integrated circuit context (e.g. processor state) intact may be significantly less than the voltage at which the processor can functionally operate at a particular frequency, significant power savings can be achieved by reducing processor voltage while the processor clocks are stopped.

In one embodiment, the invention provides a method of supplying a first voltage to at least a first circuit portion of an integrated circuit during an operational mode. The method further includes stopping clocks which are being supplied to the first circuit portion to place the integrated circuit in a reduced power consumption state and then supplying a second voltage, less than the first voltage, to the first circuit portion while the clocks are stopped, the second voltage being at a voltage sufficient to maintain context of the first circuit portion in existence at a time when the clocks were stopped.

In another embodiment, the invention provides an apparatus that includes an integrated circuit that has a plurality of circuits holding, at least in substantial part, context indicative of a current operational state of the integrated circuit. A power supply circuit supplies variable voltages to the integrated circuit. A control circuit is coupled to the power supply circuit, and supplies the power supply circuit with first voltage control information, indicating a first voltage to be supplied, while clocks are being supplied to the plurality of circuits. The control circuit supplies the power supply circuit with second voltage control information, indicating a second voltage to be supplied, while the clocks are stopped, the second voltage being lower than the first voltage.

BRIEF DESCRIPTION OF DRAWINGS

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings, wherein:

Fig. 1 illustrates an exemplary system that can exploit the present invention;

Fig. 2 illustrates additional details over a control circuit used in one embodiment of the present invention; and

Fig. 3 is a flow chart of an embodiment of the present invention.

MODE(S) FOR CARRYING OUT THE INVENTION

Additional power savings can be realized in computer systems by reducing the voltage supplied to the processor during a state in which processor clocks are stopped and processor context is maintained. With the

clocks off, the voltage level required to maintain processor context can be reduced to levels below that needed for proper operation of the clocked circuits. Put another way, the voltage required to maintain state, is lower than that needed to change state reliably.

In an exemplary embodiment illustrated in Fig. 1, voltage regulator 101 supplies core voltage 102 to processor (CPU) 103. In the embodiment illustrated, integrated circuit 105 controls the voltage level that is supplied to CPU 103 by supplying voltage control signals VID[0:4] to voltage regulator 101. VID refers to "voltage ID" which is commonly used in the industry to describe the voltage control signals. Integrated circuit 105 may be a south bridge integrated circuit, which is known in the art as one chip of a chipset pair. The south bridge, originally providing a bridge between the Peripheral Component Interconnect (PCI) bus and the ISA bus, also typically incorporates power management functions. The south bridge may also contain integrated legacy functions, as well as interfaces for newer buses such as Universal Serial Bus (USB) and other additional functions. The chipset pair also typically includes a north bridge integrated circuit (not shown) that provides a memory control function as well as a bridge function between the host bus connected to the processor and the Peripheral Component Interconnect (PCI) bus. Clock generator 107 supplies a clock signal 106 used by CPU 103 to generate clocks supplied to core logic in the processor. Clock generator 107 can be controlled by clock stop signal 112 to selectably turn on and off clocks supplied to CPU 103 and other system components.

The variable voltage regulator 101 may be, e.g., the National Semiconductor's LM4130, whose output voltage can be controlled by an external device such as south bridge 105. It is desirable for the voltage regulator to support at least four control bits and for the output voltage to be controllable in steps of 50mV (or smaller) covering a minimum range of from 1.45 to 2.2 volts. A wider range or different granularity may be desirable in some applications.

The CPU clocks can be stopped as follows. The "stop clock" signal refers to STPCLK# signal 110 (where # indicates an active low signal), which causes CPU 103 to stop execution at the end of the current instruction, and turn off internal distribution of the CPU's clock, to most, if not all sections of processor core logic. The CPU executes a "Stop Grant" bus cycle to indicate that the CPU has entered the Stop Grant state.

In addition to stopping distribution internally, clocks to the CPU and other components may be stopped using the "clock stop" signal 112 provided by south bridge 105 to clock generator 107. One typical sequence to stop the clocks is to assert the STPCLK# signal 110 to enter the Stop Grant state, wait for the Stop Grant bus cycle and then turn off the clock generator 107 distribution of clocks using the clock stop signal 112 to enter the Stop Clock state.

Assume that the clocks to the processor are stopped as described above. The particular mechanism to stop clocks may vary in different embodiments and is not critical to the present invention. The clocks may be stopped in association with throttling or because of the processor entering a sleep mode or any other scenario in which clocks are stopped and power is left on. After the clocks are stopped, the south bridge 105 (or any other suitable logic device) supplies new voltage control signals to the CPU core voltage regulator 101 instructing the voltage regulator to supply a reduced voltage to the CPU core. Depending on the sleep mode, it

may still be important that the voltages supplied to other areas of the CPU, such as the I/O circuits are maintained at suitable levels since such circuits may be interfacing with I/O devices, external circuits or buses that may be active when the processor has its core logic clocks stopped.

Because sleep and throttle (and suspend) states require the processor operation to be stopped, it is impossible for system software to control all sleep, and recover operations. To overcome this problem, control logic is typically implemented external to the processor. For example, such control logic may be implemented in the input/output integrated circuit (referred to herein as south bridge 105) to control the final stages of sleep and suspend operations and the resume operation and other common power management features. One such integrated circuit is the Intel Corp. 82371AB PCI-TO-ISA/IDE XCELERATOR (PIIX4). The power management features contained therein reduce power consumption to extend battery life and control heat generation and dissipation to safely operate the processor. While some computer systems use a separate microcontroller for the task, most computer systems, including most notebook computers rely on the south bridge to provide the hardware needed for controlling thermal and power management. South bridge chips from various manufacturers have typically utilized the registers, timers and state machine definitions used in the Intel PIIX4 South Bridge. PIIX4 compatibility in current south bridge chips can be extended to support managing the core voltage during sleep states as described herein.

The control logic to reduce the core voltage after the clocks are turned off may be implemented as a state machine in south bridge 105. It may be particularly advantageous to augment or modify existing power management control logic in the south bridge to provide the enhanced functionality described herein. Once the voltage to the core has been reduced, the control logic waits for a system event that causes the CPU to resume processing. In the meantime the processor is in a quiescent state with the current consumption lower than it otherwise would have been. The system event causing the processor to wake-up, such as mouse movement or depressing a keyboard key, causes the CPU to resume normal operations. The control logic ensures that the core voltage is returned back to an operational level sufficient to support the desired clock frequency prior to the clocks being turned on. Otherwise, unpredictable results may be caused by clocking circuits when the power supply voltage is too low. Thus, the control logic issues new voltage control settings to voltage regulator 101 corresponding to a desired frequency and then the clocks are turned back on by, e.g., enabling clocks at clock generator 107, if necessary, and deasserting STPCLK#.

For a particular processor, the minimum operating core voltage ($V_{coremin}$), which specifies the minimum operating voltage required and the minimum static core voltage ($V_{coremins}$), which specifies the voltage necessary to maintain context with clocks stopped, can be specified over the entire product line. In one embodiment, the voltage control signal (VID) settings corresponding to $V_{coremin}$ and $V_{coremins}$ may be built into BIOS tables. When the system management software determines that the system needs to be put into a mode where clocks are stopped (e.g., a sleep mode or a throttle clock state), the core voltage is reduced to $V_{coremins}$ after the clock has been stopped. Note that if clocks are stopped externally, it may also be possible to reduce the voltage being supplied to I/O regions of the processor under some circumstances. When the system needs to be restored to operating conditions, the system automatically increases the core voltage to the setting needed

for the CPU operation at the desired frequency using the VID settings in the BIOS tables. The control settings may of course be located in any suitable location in the computer system.

Power savings will vary according to the leakage current present in the particular integrated circuit. For example, a processor consuming hundreds milliwatts of power while clocks are stopped in the Stop Grant state (on chip clock multiplier logic is still active) might reduce leakage current by lowering the power supply voltage enough to reduce power consumption by approximately 10%.

The voltage regulator's control pins should be configured for appropriate default operation upon power-up. Accordingly, as shown in Fig. 1, south bridge 105 in one embodiment, has jumper inputs IV[4:0]. The settings of the jumpers 111 (open or short), along with resistors 113, determine the default values for the VID signals. The IBF[2:0] inputs are for frequency control and a description of their use is not critical to understand the present invention. In addition to default modes, the south bridge 105 (or other suitable circuit) supplies the voltage regulator 101 with appropriate voltage control settings during operational modes and during sleep modes in which processor context is maintained.

Referring to Fig. 2, a high level block diagram shows one approach an integrated circuit (such as the south bridge in current x86 based computer systems) may use to provide appropriate voltage control settings for voltage regulator 101 (Fig. 1). In the embodiment illustrated in Fig. 2, multiplexer 201 receives three voltage controls settings as inputs. The first voltage control setting is from VID jumper settings 111, which as previously described, provide for default voltage settings on power-up. Multiplexer 201 also receives inputs from VID stop clock register 202, which provides the voltage control setting for the reduced processor voltage during stop clock modes ($V_{coremins}$). Multiplexer 201 receives inputs from VID operational register 203, which provides VID values for operational modes of the processor, i.e., when core clocks are running. Multiplexer 201 selects between the various voltage control settings according to a select line 204 supplied by control logic 210. Control logic 210 receives reset signal 207 and selects the jumper settings as the appropriate voltage control settings when reset (power on or other hard or soft reset) is asserted. Control logic 210 also receives a stop clock signal 208 which indicates that the processor has or is about to enter a stop clock state with core power maintained. In addition, control logic 210 receives indication 209 that a wakeup event has occurred, i.e., that the processor is going to resume normal operation.

The control logic also supplies load signal 211 to output register 205. During regular operational modes in which clocks are running, multiplexer 201 selects the operational VID register 203. Note that register 203 may be programmable to provide various VID signals during various operational modes. When the processor is in a sleep or throttle mode in which clocks are stopped, the control logic selects the VID stop clock register settings as the source for the voltage control signals VID. Thus, after the clocks are stopped (or simultaneously therewith), the select line selects the VID values from the stop clock VID register 202. The control logic then waits for a wake-up event to occur. When the wake-up event occurs as indicated by wake up signal 209 and before the clocks are started, the control logic causes the operational voltage control signals corresponding to the desired frequency of operation to be loaded into output register 205 from VID operational register 203. The clocks may then be enabled.

A variety of other circuit implementations would be readily apparent to one of skill in the art to accomplish the function of the circuit illustrated in Fig. 2. For example, the multiplexer may only select between jumper settings and a VID register with the VID register being appropriately updated before values in the register are supplied to the voltage regulator 100. That is, south bridge 105 can utilize a programmable register that can be written to update the VID pins with the appropriate voltage control settings available from, e.g., the BIOS tables rather than have separate operational and stop clock registers.

Referring to Fig. 3, a flow chart illustrates the operation of a system incorporating one embodiment for controlling core voltage to effectuate greater power savings according to the present invention. Assume that the clocks are stopped in 301. The clocks may be stopped using the STPCLK# signal 110 or using clock stop signal 112 to turn off the clock signal 106 being supplied to the processor clock multiplier logic, or both, or in any other manner appropriate for the particular implementation. After the clocks are stopped, the system reduces the core voltage being supplied to processor core logic in 303. That is accomplished, e.g., by selecting the appropriate voltage control settings and supplying those settings to the CPU core voltage regulator. Once the processor is maintaining its context with the reduced core voltage, and thereby realizing greater power savings, the control logic waits for a wake-up event in 305. Once the wake-up event occurs, the core logic voltage is changed to a level corresponding to the desired frequency of operation in 307 and then, after the processor is receiving the higher voltage, the clocks are turned on and the processor resumes normal operation.

The description of the invention set forth herein is illustrative, and is not intended to limit the scope of the invention as set forth in the following claims. For instance, while this invention has been described with relation generally to x86 based computer systems and is particularly relevant to notebook computers (which may also be referred to as laptops, portable or mobile computers), the teachings herein may also be utilized in any computing device such as personal digital assistants (PDAs), as well as systems containing any variety of processor in which it is desirable to save power by reducing voltage while clocks are stopped in a power savings mode and still maintain context. Further, while the description herein has focused on reducing core voltages in processors or CPUs, the power savings is equally applicable to any integrated circuit in which clocks are stopped to save power while context is maintained. Other variations and modifications of the embodiments disclosed herein, may be made based on the description set forth herein, without departing from the scope and spirit of the invention as set forth in the following claims

WHAT IS CLAIMED IS:

1. A method comprising:

supplying a first voltage to at least a first circuit portion of an integrated circuit during an operational mode;

stopping clocks which are being supplied to the first circuit portion to place the integrated circuit in a reduced power consumption state; and

then supplying a second voltage, less than the first voltage, to the first circuit portion while the clocks are stopped, the second voltage being at a voltage level sufficient to maintain context of the first circuit portion in existence at a time when the clocks were stopped.

2. The method as recited in claim 1 wherein the integrated circuit is a microprocessor including core logic, the first circuit portion being the core logic.

3. The method as recited in claim 1 further comprising:

supplying a third voltage to the integrated circuit after supplying the integrated circuit with the second voltage, the third voltage being greater than the second voltage; and

then starting the clocks being supplied to the first circuit portion to resume integrated circuit operations.

4. The method as recited in claim 3 wherein the first and third voltages are equal.

5. The method as recited in claim 3 wherein the third voltage is supplied in response to a wake-up event.

6. A computing device comprising:

an integrated circuit including a circuit region holding, at least in substantial part, context indicative of a current operational state of the integrated circuit;

a power supply circuit responsive to control inputs to supply variable voltages to the integrated circuit;

a control circuit coupled to the control inputs of the power supply circuit, wherein the control circuit supplies the control inputs with first voltage control information, indicating an operational voltage, while clocks are being supplied to the circuit region and the control circuit supplies the control inputs with second voltage control information indicating a second voltage, while the clocks are stopped, the second voltage being lower than the operational voltage.

7. The computing device as recited in claim 6 wherein the operational voltage is at a voltage level required to clock the circuit region at a predetermined frequency and the second voltage is below the voltage level required to clock the circuit region at the predetermined frequency.

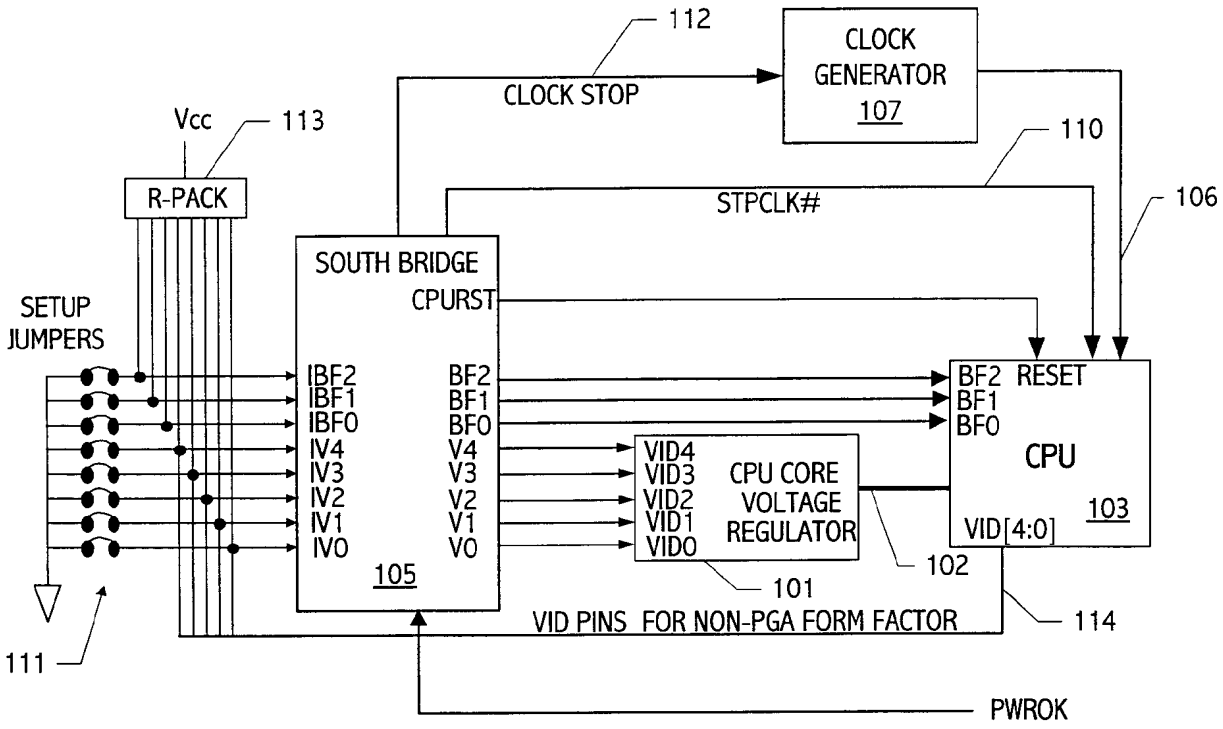
8. An integrated circuit comprising:

a logic circuit responsive to an indication of normal clock operation in which internal clocks are running, to selectably provide first voltage control information indicative of a first voltage level and responsive to an indication of a stop clock state in which internal clocks are stopped to provide second voltage control information indicative of a second voltage level, the second voltage level being lower than the first voltage level; and

an output circuit coupled to receive the selectably provided first and second voltage control information, the first and second voltage control information for coupling to control inputs of a voltage generator.

9. The integrated circuit as recited in claim 8 wherein the logic circuit includes a selector circuit coupled to selectably provide to the output circuit the first or second voltage control information as the control inputs of the voltage generator and further includes at least a first programmable register coupled to the selector circuit and holding at least one of the first voltage control information and the second voltage control information.

10. The integrated circuit as recited in claim 9 further comprising control logic coupled to receive an indication of a wake-up event, an indication of a reset and an indication of the clock stop state, and generating a select signal for the selector circuit in response thereto.


112
CLOCK STOP
CLOCK GENERATOR
107
Vcc
113
110
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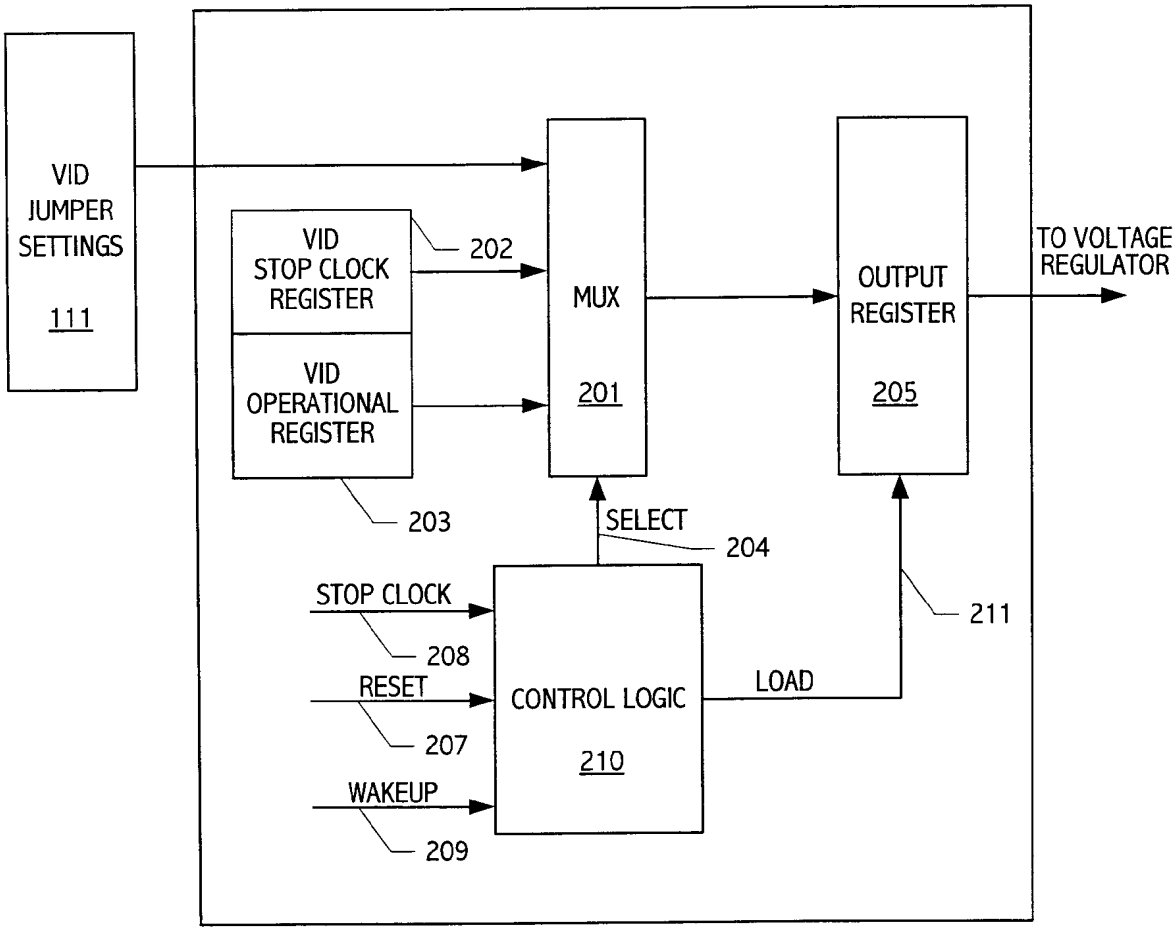
STPCLK#
106
SOUTH BRIDGE
CPURST
SETUP JUMPERS
IBF2
IBF1
IBF0
IV4
IV3
IV2
IV1
IV0
105
BF2
BF1
BF0
V4
V3
V2
V1
V0
VID4
VID3
VID2
VID1
VID0
CPU CORE VOLTAGE REGULATOR
101
102
BF2 RESET
BF1
BF0
CPU
103
VID[4:0]
111
VID PINS FOR NON-PGA FORM FACTOR
114
PWROK

FIG. 1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MUX
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OUTPUT
REGISTER
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TO VOLTAGE
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WAKEUP
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CONTROL LOGIC
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LOAD
211

FIG. 2

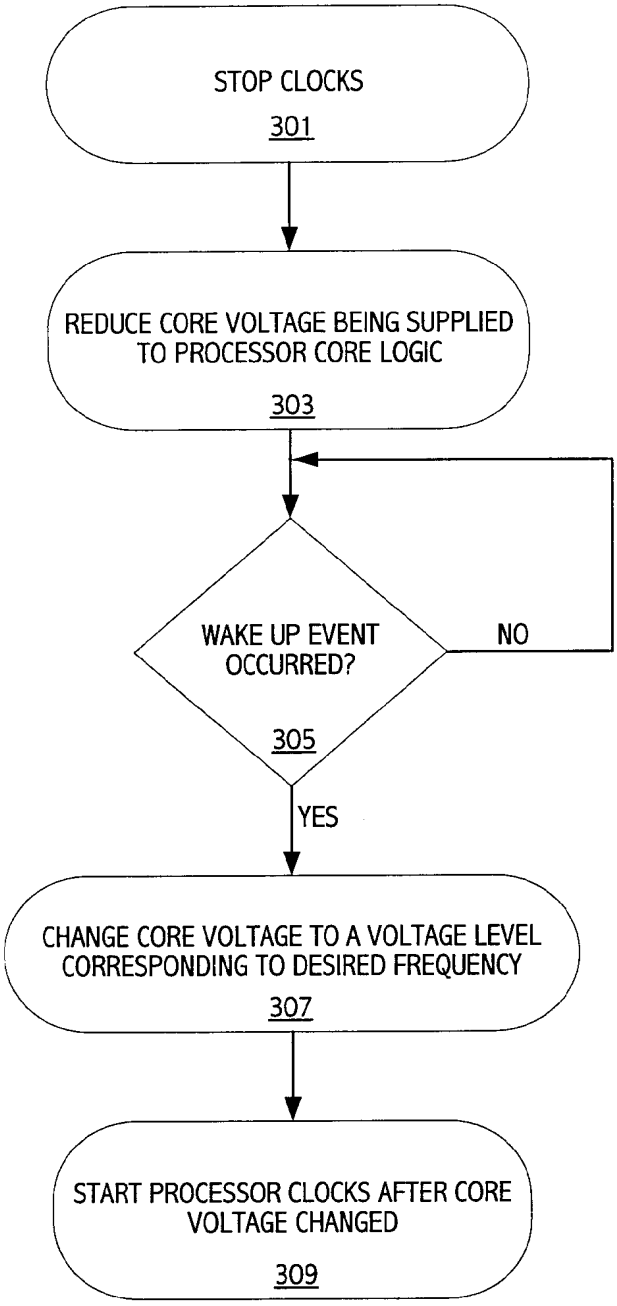
STOP CLOCKS
301
REDUCE CORE VOLTAGE BEING SUPPLIED TO PROCESSOR CORE LOGIC
303
WAKE UP EVENT OCCURRED?
305
NO
YES
CHANGE CORE VOLTAGE TO A VOLTAGE LEVEL CORRESPONDING TO DESIRED FREQUENCY
307
START PROCESSOR CLOCKS AFTER CORE VOLTAGE CHANGED
309

FIG. 3

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/US 00/11062

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F1/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 745 375 A (GUNTHER STEPHEN H ET AL) 28 April 1998 (1998-04-28) column 1, paragraph 3 column 5, paragraph 2 figure 5	1-10
X	EP 0 632 360 A (XEROX CORP) 4 January 1995 (1995-01-04) column 4, paragraph 2 column 7, paragraph 3 figures 1-3	1-10
X	US 5 852 737 A (BIKOWSKY ZEEV) 22 December 1998 (1998-12-22) column 3, line 20 - line 38 column 7, paragraph 2; figures 2,3,6	1-10

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 September 2000	22/09/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Ciarelli, N

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte onal Application No
PCT/US 00/11062

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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